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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,051	03/11/2004	Giovanni Gilardi	AVAN/001112	6732

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EXAMINER	
CHIEM, DINH D	
ART UNIT	**PAPER NUMBER**
2883	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,051	GILARDI ET AL.	
	Examiner	Art Unit	
	Erin D. Chiem	2883	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-18 and 20-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-18 and 20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Brian Healy
Primary Examiner

DETAILED ACTION

This office action is in response to the amendment filed on October 14, 2005. Claims 8 and 19 are canceled, claims 21 and 22 are new, and currently claims 1-7, 9-18, and 20-22 are pending.

In view of the amendment and remarks the drawing objection is withdrawn as well as the objection made to claims 2-7, 13-16, and 18.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-5, 7, 9-12, 14-16, 18, and 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishimura et al. (US 5,602,672 hereinafter "Ishimura").

Regarding claims 1, 9-11, Ishimura teaches a light modulator module comprising a semiconductor modulator chip (Fig. 6; 1) and a microwave input chip (3), formed of alumina, coupled to the modulator chip having a thin film resistor (5).

Regarding claims 3-5 and 14-16, Ishimura further teaches the microstrip line in the microwave input chip (3) and the thin film resistor (5) being placed in the microstrip line; wherein the microstrip line is a straight line. The recitation of "the microwave input chip" is defined in the Specification in the Summary of Invention on page 4 paragraph [0007]. Applicant

defines the microwave input chip is a microwave thin film resistor on an accessory connection chip located between the RF connector of the microwave input and the RF electrode of the Lithium Niobate chip, thus, Ishimura's chip (3) meets the definition of the microwave input chip without explicitly disclosing in the similar terms. Furthermore, the coplanar waveguide is an alternative term in the art referring to the microstrip; the type of waves that the microstrip guides is a microwave.

Regarding claims 7 and 18, the modulator chip 1 is bonded by the bonding pad 21, 22, and the wire 10.

Regarding claim 12, employing lumped resistance is implicitly anticipated by Ishimura. In Figure 1(b), clearly the network analysis disclosure implies that conventional lumped resistor maybe employed. However, Ishimura further teaches the improvement of impedance matching by employing a thin-film resistor since the resistance is easily controllable by increasing or decreasing the controlling signal to the thin-film resistor. Prior to the knowledge of thin-film resistor, lumped resistors are used, therefore, it is necessary that if without the thin-film resistor, lumped resistor must be used to provide impedance in the network.

Regarding claim 21 and 22, thin film resistors are routinely function in the low resistance range since high resistance will easily damage the resistors. Thus it is understood in the art that thin film resistors are made in the range of a few ohms.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishimura in view of Roxlo (US 4,863,245 hereinafter "Roxlo"). Ishimura teaches light modulator module comprising a semiconductor modulator chip (Fig. 6; 1) and a microwave input chip (3), formed of alumina, coupled to the modulator chip having a thin film resistor (5).

However, Ishimura does not explicitly teach the modulator is formed of lithium-niobate. however, Lithium Niobate is a well-known semiconductor compound.

Roxlo teaches a superlattice electrooptic device having a superlattice layer modulator (Fig. 11 (62)). The modulator is made of lithium-niobate for the purpose of integrating with other opto-electronics by depositing the lattice as a layer onto the same chip as a laser diode (col. 11, lines 3-13).

Since Ishimura and Roxlo are both from the same field of endeavor, the purpose disclosed by Roxlo would have been recognized in the pertinent art of Ishimura.

It would have obvious to one having ordinary skill in the art to integrate the laser diode and the modulator onto a single chip from the teaching of Roxlo. **The motivation** for forming the modulator from lithium-niobate is for its superlattice properties that allows one having ordinary skill in the art to deposit it onto a substrate as a thin layer at a low temperature without lattice matching constraints.

Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishimura In applicant's disclosure [0019], the limitation of the curved path microstrip line was taught as a design choice since there applicant does not further disclose the advantage or significance of the

coplanar line comprises a curved line. **The motivation** for implementing a curved coplanar line instead of a straight coplanar line is that applicant does not have chip surface area constraint in the design process. Examiner's contention of this obvious choice in design can be overcome if applicant establishes unexpected results between curved and straight path microstrip lines as claimed.

Response to Arguments

Applicant's arguments filed on October 14, 2005 have been fully considered but they are not persuasive. Applicant's main argument is that Ishimura does not teach a microwave input chip. The examiner demonstrated in the above rejection that based on applicant's definition of the microwave input chip on page 4 of the Specification defines the chip as an accessory connection chip wherein a microwave thin film resistor is placed upon and the chip is located between the connector of the waveguide input and the Lithium Niobate chip. Thus Ishimura teaches the microwave input chip. Applicant is silent on the rejection made to other claims, therefore the examiner maintain the previous rejection made in prior office action with mail date June 14, 2006.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin D. Chiem whose telephone number is (571) 272-3102. The examiner can normally be reached on Monday - Thursday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank G. Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erin D Chiem
Examiner
Art Unit 2883

Brian Healy
Primary Examiner